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MEC COMPANY LTD.

U.S.–Japanese Consortium "US-JOINT" Begins Full-Scale Development of Next-Generation Semiconductor Packages

Union City, CA, USA (April 20, 2026) MEC COMPANY LTD. today announced the establishment of a new R&D center to mark the full-scale launch of “US-JOINT,” a consortium comprising 12 Japanese and U.S. materials and equipment manufacturers, with the goal of establishing new models for developing next-generation semiconductor-packaging technologies. To commemorate the occasion, a ceremony attended by government officials and participating companies from both countries was held at the consortium's newly operational base in Silicon Valley on April 20.

The new R&D center is the first in the United States dedicated to developing advanced semiconductor-packaging technologies. The consortium will leverage this R&D base in Silicon Valley to validate new concepts in collaboration with major users of advanced semiconductors. By capturing market needs in real time and combining the technological capabilities of leading Japanese and U.S. manufacturers of materials and equipment, the consortium will accelerate the research and development of materials, evaluation and packaging technologies to enable the rapid commercialization and deployment.

Hidehito Takahashi, President and CEO of Resonac, commented: "US-JOINT aims to shorten the proof-of-concept (PoC) period from approximately six months to as little as one month by enabling 12 participating Japanese and U.S. companies to conduct development in Silicon Valley, home to major hyperscalers. Through “collaboration” between semiconductor-related companies from Japan and the United States, the initiative will accelerate global semiconductor innovation."

Resonac will leverage US-JOINT's technological foundation and knowledge to play a central role in promoting co-creation while overseeing the consortium. As a materials manufacturer with a comprehensive understanding of the entire semiconductor manufacturing process, Resonac will bring together the technologies and ideas of participating companies to contribute to concept validation and accelerate co-creation targeted at market needs.

Dilip Vijay, Vice President and Head of Global IC Operations, Broadcom Inc., commented: "A collaborative effort like US-JOINT is exactly what the industry has needed. I am very much looking forward to the US-JOINT R&D center's full-scale operation in Silicon Valley. We expect this initiative to speed up semiconductor innovation and spark entirely new breakthroughs beyond what we see today."

Raja Swaminathan, Vice President of Heterogeneous Integration Technologies, Advanced Micro Devices, Inc., said: "With US-JOINT now fully operational in Silicon Valley, we expect face-to-face technical dialogue to lead to more efficient joint development through faster feedback and clearer understandings. We welcome US-JOINT’s efforts and look forward to the innovations and strengthened ecosystem collaboration this initiative can enable."

Kazumi Nishikawa, Director-General for Economic Security Policy, Trade and Economic Security Bureau, Ministry of Economy, Trade and Industry, remarked: “The expansion of generative AI and the current requirements of computing demands more advanced packaging. I am very confident that US-JOINT is just the start of innovation for advanced packaging and chiplets in generative AI computing. Finally, I truly appreciate the effort that led to today, and I hope that today's one step can lead to a tremendous outcome for the U.S. and Japan and to the world.”

Overview of US-JOINT

Name	US-JOINT (JOINT: Jisso Open Innovation Network of Tops)
Objectives	To create an evaluation platform for next-generation semiconductor packaging and develop packaging technology in the United States.
Participants (alphabetical order)	12 companies (as of April 20, 2026) Resonac Corporation; Azimuth Industrial; KLA Corporation; Kulicke and Soffa Industries; MEC Co., Ltd.; Moses Lake Industries; Namics Corporation; Tokyo Ohka Kogyo Co., Ltd.; Toppan Inc.; TOWA Corporation; ULVAC, Inc.; and The 3M Company
Location	Union City, California, USA
Launch	April 2026 (full-scale operation)
Main Facilities/Environment	Advanced semiconductor packaging processes (patterning, bonding, molding, plating, etc.), evaluation and analysis equipment, cleanrooms (Classes 100 and 1,000).
Facility Role	R&D center for validating next-generation semiconductor-packaging concepts.
Intended Users	Fabless companies, semiconductor manufacturers, and engineers from participating companies.

MEC's Role in US-JOINT

The company provides essential solutions for the copper-resin interlayer adhesion process in semiconductor package substrate manufacturing, holding a top global market leader. In addition to the expertise in chemical development for electronic substrates that we have cultivated since our founding, our high level of technical capability and solution-providing capacity represent our greatest strengths. Through our participation in US-JOINT, we aim to leverage the metal surface treatment technology and knowledge we have honed over the years to accelerate technological innovation and advancement in the semiconductor industry in the United States. Furthermore, we will collaborate with domestic and international participating companies with high technological capabilities to contribute to the creation of new value. We are confident that our activities within this consortium will support the evolution of next-generation semiconductor packaging technology and contribute to the development of a digital society and the building of a sustainable society.